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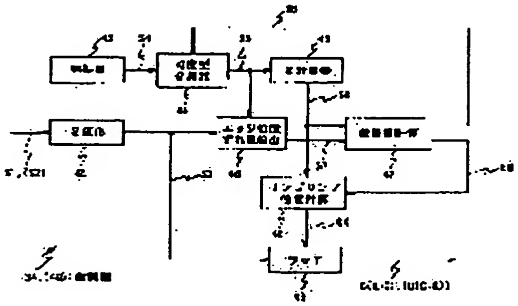
(54) PLL CIRCUIT, DEMODULATION CIRCUIT, IC CARD AND IC CARD PROCESSING UNIT

(57)Abstract:

PROBLEM TO BE SOLVED: To surely process with a simple configuration an input signal, even when the deteriorated input signal is received by applying a PLL circuit and a demodulation circuit to the IC card that receives/outputs various data, for example, with out making contact, and to the IC card processing unit that makes data communication with the IC card with respect to the PLL circuit, the demodulation circuit, the IC card and the IC card processing unit.

SOLUTION: The phase shift of a leading edge a trailing edge is calculated by selectively averaging phase comparison results S7 to be an oscillated output signal S5 and a binary signal S3, the phase shift is used to control an oscillated output signal S6, a control direction is decided, based on the polarity of a phase comparison result between oscillation output signals with a phase difference of 90 degrees, and the oscillated output signal is controlled in this control direction.



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention is applicable to the IC card processor which carries out data communication to the IC card which outputs and inputs various data according to non-contact, and this IC card, concerning a PLL circuit, a demodulator circuit, an IC card, and an IC card processor. By this invention's calculating the amount of phase shifts to which at least that of an oscillation output signal and a binary-ized signal average-value-izes a phase comparison result selectively, and receives any of a rising edge or a falling edge they are, and controlling an oscillation output signal from this amount of phase shifts Moreover, even when an input signal deteriorates, it enables it to process an input signal certainly with a simple configuration by determining the control direction on the basis of the positive/negative of a phase comparison result to the extent that it is based on the oscillation output signal with which phases differ about 90 degrees, and controlling an oscillation output signal in this control direction.

[0002]
[Description of the Prior Art] Conventionally, in IC card system using an IC card, it is made as [apply / to the ticket gate system of a means of transportation, the close recession managerial system of a chamber, etc.]. Such an IC card system is constituted by the lead writer (that is, it becomes with an IC card processor) which sends and receives data various between the IC card which a user carries, and these IC cards, and what was made as [receive / various data / between these IC cards and a lead writer / according to non-contact / send and] is proposed.

[0003] That is, in this kind of IC card system, it becomes irregular by the data stream of a request of the subcarrier of predetermined frequency, and a lead writer generates a sending signal, and sends out this sending signal to an IC card.

[0004] An IC card receives this sending signal through an antenna, and restores to the data sent out from the lead writer from this sending signal. Furthermore, an IC card modulates data, such as individual humanity news held inside, by the predetermined subcarrier according to this received data, and sends them out to a lead writer.

[0005] The lead writer is made as [permit / receive the data sent out from this IC card, and open and close the door of a ticket gate machine from this received data, and / close recession of a chamber].

[0006] In such an IC card system, it is made as [receive / the data which received the data sent out from the lead writer using the demodulator as shown in drawing 11 , and were transmitted from the IC card].

[0007] That is, this demodulator 1 inputs into the binary-ized circuit 2 of limiter circuitry the PSK modulating signal S1 recovered from the antenna input, and makes the PSK modulating signal S1 binary here. The phase comparison circuit 3 is constituted by the IKUSUKURUSHIBUOA circuit which carries out the phase comparison of the clock CK outputted from the control mold oscillator circuit 4 to the binary-ized signal SA outputted from this binary-ized circuit 2, and outputs a phase comparison result to a low pass filter (LPF) 5. A low pass filter 5 band-limits a phase comparison result, and generates the control signal of the control mold oscillator circuit 4. The control mold oscillator circuit 4 carries out adjustable [of the oscillation frequency] according to this control signal.

[0008] Thereby, a demodulator 1 generates the clock CK which constituted the PLL circuit and carried out phase simulation to the binary-ized signal SA, and reproduces Clock CK from an PSK modulating signal. A latch circuit 6 carries out the sequential latch of the binary-ized signal with this clock CK, and is made as [output / the data stream D1 which comes to get over the PSK modulating signal S1 by this].

[0009]

[Problem(s) to be Solved by the Invention] By the way, in IC card system, an antenna input changes with the distance of an IC card and a lead writer a lot. In connection with this, the wave of the PSK modulating signal S1 deteriorates remarkably in the PSK modulating signal by the Manchester code etc., and a S/N ratio also deteriorates greatly.

[0010] When it becomes such, a duty ratio changes in the binary-ized signal acquired by making the PSK modulating signal S1 binary, and the conventional demodulator has the problem to which it becomes difficult for this to reproduce the clock of the PSK modulating signal S1 correctly from the binary-ized signal SA. Thus, if it becomes difficult to reproduce a clock correctly, it will also become difficult to carry out data playback that much correctly.

[0011] As one approach of solving this problem, how to restore to an PSK modulating signal by the Costas loop formation can be considered. However, the Costas loop formation has a fault with it difficult [to apply] by processing an PSK modulating signal by analog signal processing in the IC card with which a simple configuration is called for.

[0012] This invention was made in consideration of the above point, it is a simple configuration, and even when an input signal deteriorates, it tends to propose the PLL circuit which can process an input signal certainly, a demodulator circuit, the IC card which used these, and an IC card processor.

[0013]

[Means for Solving the Problem] In order to solve this technical problem, it sets to this invention. The 1st amount of phase shifts of a binary-ized signal [as opposed to / in a PLL circuit, average-value-ize a phase comparison result selectively to the extent that it is with an oscillation output signal and a binary-ized signal, and / the rising edge of an oscillation output signal], The 2nd amount of phase shifts of the binary-ized signal over the falling edge of an oscillation output signal is calculated. From this 1st or 2nd amount of phase shifts, the control signal which controls the frequency of an oscillation output signal is outputted, further, based on the detection result of the 2nd or 1st amount of phase shifts, the phase of an oscillation output signal is amended and a clock is outputted.

[0014] Moreover, in a demodulator circuit, the sequential latch of the binary-ized signal is carried out with this clock.

[0015] Moreover, in an IC card and an IC card processor, a data stream is recovered from the sending signal received by the previous demodulator circuit through the antenna.

[0016] It applies to a PLL circuit. At least that [1st] of the 1st oscillation output signal and a binary-ized signal Moreover, a phase comparison result, A phase comparison result is obtained, at least those [these / 1st and 2nd] determines the control direction based on the positive/negative of a phase comparison result, and at least that [2nd] of the 2nd oscillation output signal with which phases differ about 90 degrees to this 1st oscillation output signal, and said binary-ized signal controls actuation of a signal generation means based on this control direction.

[0017] Moreover, in a demodulator circuit, at least that [this / 1st or 2nd] outputs said data stream by the phase comparison result.

[0018] Moreover, in an IC card and an IC card processor, a data stream is recovered from the sending signal received by the previous demodulator circuit through the antenna.

[0019] In a PLL circuit, if a phase comparison result is selectively average-value-ized to the extent that it is with an oscillation output signal and a binary-ized signal, and the 1st [of the binary-ized signal over the rising edge of an oscillation output signal] amount of phase shifts and the 2nd amount of phase shifts of the binary-ized signal over the falling edge of an oscillation output signal are calculated, the 1st and 2nd amounts of phase shifts can be calculated by the ability to avoid the effect by the noise. Moreover, if the control signal which controls the frequency of an oscillation output signal from this 1st or 2nd amount of phase shifts is outputted, even when the duty ratio of a binary-ized signal will change, an oscillation output signal can be controlled so that any of the rising edge of an oscillation output signal or a falling edge they are carries out phase simulation to a binary-

ized signal. If the phase of an oscillation output signal is amended and a clock is outputted based on the detection result of the 2nd [which remains by this], or 1st amount of phase shifts, the clock of an input signal is reproducible.
[0020] Thereby, even when carrying out the sequential latch of the binary-ized signal with this clock in the demodulator circuit and an input signal deteriorates, it can restore to the data transmitted by the input signal certainly.
[0021] Moreover, in an IC card and an IC card processor, even when recovering the data stream from the sending signal received by the previous demodulator circuit through the antenna, and the distance between an IC card and an IC card processor changes and a sending signal deteriorates, data can be received certainly.
[0022] Moreover, it applies to a PLL circuit and a value changes [in / at least in that / 2nd / of the 2nd oscillation output signal with which phases differ / as opposed to / at least in that / 1st / of the 1st oscillation output signal and a binary-ized signal / a phase comparison result and this 1st oscillation output signal / about 90 degrees, and said binary-ized signal / a phase comparison result] with the variation rates of the frequency of the oscillation output signal over the clock of a binary-ized signal. Furthermore, the value of this phase comparison result will change corresponding to the phase contrast of the 1st oscillation output signal and the 2nd oscillation output signal. Phase simulation only of that [1st or 2nd] can be carried out by this, using a phase comparison result selectively, and at least that [this / 1st or 2nd] can detect the change rate of a sign by the positive/negative of a phase comparison result. If at least those [these / 1st and 2nd] determines the control direction based on the positive/negative of a phase comparison result and controls actuation of a signal generation means based on this control direction by this, phase simulation of the 1st oscillation output signal or the 2nd oscillation output signal can be carried out to a clock. If at least those [1st and 2nd] determines the control direction based on the positive/negative of a phase comparison result and controls actuation of a signal generation means based on this control direction at this time, phase simulation can be carried out by the simple configuration.
[0023] Thereby, in a demodulator circuit, at least that [this / 1st or 2nd] outputs a data stream by the phase comparison result, and it can restore to the data transmitted by the input signal simply and certainly.
[0024] Moreover, in an IC card and an IC card processor, even when recovering the data stream from the sending signal received by the previous demodulator circuit through the antenna, and the distance between an IC card and an IC card processor changes and a sending signal deteriorates, data can be received certainly.
[0025]
[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained in full detail, referring to a drawing suitably.
[0026] (1) Gestalt drawing 2 of the 1st operation is the block diagram showing IC card system concerning the gestalt of operation of the 1st of this invention. This IC card system 11 is applied to the ticket gate system of a means of transportation, and carries out the data exchange to IC card 12 between the lead writers 13.
[0027] IC card 12 carries out the laminating of the substrate and protection sheet which mounted the integrated circuit, and is formed in the shape of a card type here. As for IC card 12, a loop antenna 14 is formed with the circuit pattern on this substrate. Moreover, with the integrated circuit mounted on this substrate, the strange demodulator circuit 15 and a digital disposal circuit 16 are formed.
[0028] It combines with the loop antenna 18 of the lead writer 13, and a loop antenna 14 emits the reply signal generated in the strange demodulator circuit 15 here while receiving the sending signal sent out from this loop antenna 18.
[0029] The strange demodulator circuit 15 generates power required for actuation of this IC card 12, a clock, etc. from the sending signal which received with the loop antenna 14. Furthermore, the strange demodulator circuit 15 operates with this power and a clock, from a sending signal, restores to data stream (it is called transmit data train below) D(R->C) sent out from the lead writer 13, and outputs it to a digital disposal circuit 16. Moreover, from data stream (it is called response data stream below) D(C->R) which is urged to transmission by this transmit data train D (R->C), and is inputted from a digital disposal circuit 16, a reply signal is generated, a loop antenna 14 is driven

with this reply signal, and a reply signal is emitted.

[0030] A digital disposal circuit 16 operates with the power and the clock which were generated in the strange demodulator circuit 15, analyzes the transmit data train D (R->C), and outputs response data stream D (C->R) to the strange demodulator circuit 15 if needed.

[0031] In the lead writer 13, from the transmit data train D (R->C) inputted from SPU (signal process unit)20, the strange demodulator circuit 19 generates a sending signal, and drives a loop antenna 18 by this sending signal. Moreover, the strange demodulator circuit 19 carries out signal processing of the reply signal received with this loop antenna 18, restores to response data stream D (C->R) sent out from IC card 12, and outputs this response data stream D (C->R) to SPU20.

[0032] SPU20 processes response data stream D (C->R) which is constituted by the data-processing unit which performs comparatively simple procedure, and sends out the transmit data train D (R->C) transmitted to IC card 12 to the strange demodulator circuit 9, and is inputted from this strange demodulator circuit 19. In this processing, SPU20 displays processing progress and a processing result on a display 21 if needed. Moreover, data, such as procedure, are outputted [a switch and if needed] with the command from the input section 22 and inputted for actuation between external devices 23.

[0033] Drawing 3 is the block diagram showing the strange demodulator circuit 15 of IC card 12, and the strange demodulator circuit 19 of the lead writer 13.

[0034] In this strange demodulator circuit 19, a modulator 27 carries out the PSK modulation of the transmit data train D (R->C) inputted from SPU20 with the clock CK 1 of predetermined frequency F1, and outputs the PSK modulating signal S1 by the Manchester code. A modulator 28 carries out the ASK modulation of the PSK modulating signal S1 outputted from a modulator 27 by the main carrier Sm of predetermined frequency Fm, and drives a loop antenna 18.

[0035] The lead writer 13 modulates the transmit data train D (R->C) to two steps by these, a sending signal is generated, and this sending signal is sent out from a loop antenna 18.

[0036] In the strange demodulator circuit 15 by the side of IC card 12, the current supply circuit 29 receives the sending signal by which induction is carried out to a loop antenna 14, rectifies this sending signal, and generates DC power supply. The current supply circuit 29 supplies these DC power supply to each circuit block of IC card 12, and, thereby, operates the strange demodulator circuit 15 and a digital disposal circuit 16 with the power of a sending signal.

[0037] The carrier extractor 30 receives a sending signal from a loop antenna 14, and extracts a main carrier component from this sending signal. Furthermore this main carrier component is used as a clock of operation, and it outputs to a demodulator 32. Furthermore, the carrier extractor 30 generates various reference clocks on the basis of this clock of operation, and outputs this reference clock to digital-disposal-circuit 16 grade.

[0038] A demodulator 32 restores to the PSK modulating signal S1 of the modulator 27 to which this sending signal comes to be superimposed by receiving a sending signal from a loop antenna 14, and processing this sending signal using the clock of operation outputted from the carrier extractor 30.

[0039] A band pass filter 33 outputs selectively the signal component corresponding to the output signal S1 of a modulator 27 by band-limiting the PSK modulating signal S1 outputted from this demodulator 32.

[0040] A demodulator 34 recovers the transmit data train D (R->C) from the output signal of this band pass filter 33, and outputs this transmit data train D (R->C) to a digital disposal circuit 16. Thereby with IC card 12, it is made as [receive / the transmit data train D (R->C) sent out from the lead writer 13].

[0041] A modulator 35 receives response data stream D (C->R) sent out to the lead writer 13 from a digital disposal circuit 16, carries out the PSK modulation of this response data stream D (C->R) with the clock CK 2 of predetermined frequency F2, and outputs the PSK modulating signal S2 by the Manchester code.

[0042] It connects with the power-source line outputted from the current supply circuit 29, and a load circuit 36 changes resistance according to the output signal S2 of a modulator 25. Thereby, a load circuit 36 changes the load of the current supply circuit 29 according to an output signal S2, and changes the input impedance of the current supply circuit 29 seen from the loop antenna 14 according to an output signal S2. Thereby, induction of the load circuit 36 is carried out to a loop antenna 14, and it changes the power of the sending signal re-radiated from this loop antenna 14 according to the output signal S2 of a modulator 35.

[0043] Thus, the electromagnetic field by the main carrier Sm to which the power re-radiated is mainly the power by the main carrier Sm, and reinforcement changes from a loop antenna 14 in the perimeter of a loop antenna 14 according to the output signal S2 of a modulator 35 will be formed. Thereby, equivalent, the strange demodulator circuit 15 carries out the ASK modulation of the output signal S1 of a modulator 35 by the main carrier Sm, generates the reply signal which conveys response data stream D (C->R) to the lead writer 13, and radiates this reply signal from a loop antenna 14.

[0044] Thereby, a load circuit 36 constitutes the modulation circuit which modulates data stream D (C->R) with the current supply circuit 29 in two steps. The power-source stabilization circuit 37 stabilizes the supply voltage changed by change of a load in this way, and is outputted.

[0045] A demodulator 38 receives the reply signal by which does in this way, is generated and induction is carried out to a loop antenna 18, and restores to the output signal S2 of the modulator 35 to which this reply signal comes to be superimposed.

[0046] A band pass filter 39 outputs selectively the signal component corresponding to the output signal S2 of a modulator 35 by band-limiting the output signal of this demodulator 38.

[0047] A demodulator 40 recovers response data stream D (C->R) from the output signal of this band pass filter 39, and outputs this data stream D (C->R) to SPU20. Thereby by the lead writer 13, it is made as [receive / response data stream D (C->R) sent out from IC card 12].

[0048] Thus, in IC card 12 and the lead writer 13 which send and receive a data stream, the frequencies F1 and F2 of clocks CK1 and CK2 are set up with the frequency from which only predetermined frequency differs. Moreover, as these frequencies F1 and F2 are shown in drawing 4 , when the PSK modulating signal S1 outputted from the modulator 27 by the side of the lead writer 13 and the PSK modulating signal S2 outputted from this modulator 35 are seen on a frequency shaft, So that sideband S1U, S1L and S2U, and S2L may not overlap Moreover, when superimposed on these PSK modulating signals S1 and S2, it is set as the fully estranged frequency so that the band pass filters 33 and 39 of a simple configuration can extract the signal component of the PSK modulating signals S1 and S2, respectively.

[0049] Thereby in IC card 12 and the lead writer 13, it is simultaneously made as [carry out / in both directions / the data exchange].

[0050] Drawing 1 is the block diagram showing the demodulators 34 and 40 applied to the strange demodulator circuits 15 and 19, respectively. The explanation which attached the sign corresponding to the part which these demodulators 34 and 40 explain only the demodulator 34 by the side of IC card 12 by being identically constituted except for the point that the signals to process differ, and is different in drawing 1 about the demodulator 40 by the side of the lead writer 13, showed the IC card system 11, and overlapped is omitted. In the IC card system 11, in these demodulators 34 and 40, the PSK modulating signals S1 and S2 by the Manchester code are processed, and it restores to data streams D (R->C) and D (C->R).

[0051] In addition, a Manchester code is bit coding which a phase reverses one period of a clock according to the logical level of the data with which transmission is presented here, as shown in drawing 5 (drawing 5 (A) and (B)). The case where the edge information on clocks CK1 and CK2 is not transmitted in the PSK modulating signals S1 and S2 according to the logical level of the data with which transmission is presented by this occurs.

[0052] In the IC card system 11, when the distance between IC card 12 and the lead writer 13 estranges, the SN ratio of the PSK modulating signals S1 and S2 to which it restored will deteriorate, and waveform distortion will occur (drawing 5 (C)).

[0053] The binary-ized circuit 42 is constituted by the binary-ized circuit of limiter circuitry, makes binary the PSK modulating signal S1 inputted from a band pass filter 33, and outputs the binary-ized signal S3 (drawing 5 (D)). In this case, in the binary-ized signal S3, from 50 [%], the part and duty ratio to which the wave of the PSK modulating signals S1 and S2 was distorted will change, and will be reproduced.

[0054] An oscillator 43 oscillates one times the frequency of predetermined to the clock CK 1 of the PSK modulating signal S1, and outputs oscillation output signal S4 by the square wave signal. The adjustable mold counting-down circuit 44 carries out dividing of the oscillation output signal S4, and outputs the oscillation output signal S5 of the square wave by the twice [about] as many frequency as this to the clock CK 1 of the PSK modulating signal S1. At this time, the good transformation counting-down circuit 44 judges the positive/negative of a control signal S8 with a fixed period, and carries out adjustable [of the division ratio] one by one by this positive/negative. Two counting-down circuits 45 carry out 1 / 2 dividing of this oscillation output signal S5, and, thereby, output the oscillation output signal S6 of the square wave a frequency comes to be in agreement mostly to the clock of the PSK modulating signal S1.

[0055] By detecting the logical level of the binary-ized signal S3 on the basis of the timing of the edge of oscillation output-signal S4, the amount detector 46 of edge location gaps is the range of 1/2 period centering on each edge of the oscillation output signal S6, and it outputs the phase comparison result S7 to the extent that it comes to detect a leading phase or a delay phase to the existence of the edge in the binary-ized signal S3, and the edge of the oscillation output signal S6 one by one.

[0056] That is, in detection of the continuous logical level on the basis of oscillation output-signal S4, when the logical level of the binary-ized signal S3 is reversed, about the edge of the oscillation output signal S6 which corresponds in this case, it can be judged that an edge exists in the binary-ized signal S3. Moreover, by judging reversal of this logical level on the basis of the timing of the edge of the oscillation output signal S6, the phase to the edge of the oscillation output signal S6 can be judged. Thereby, the amount detector 46 of edge location gaps inspects the location of the edge of the PSK modulating signal S1 in the range of order quadrant period width of face on the basis of the oscillation output signal S6, and constitutes the phase comparator which outputs the existence of an edge, and the amount of gaps of an edge.

[0057] The statistic count circuit 47 between the periods which hold this phase comparison result S7 by processing the phase comparison result S7 on the basis of the oscillation output signal S6 to the extent that the sequential input was carried out, predetermined period maintenance was carried out and the phase comparison result S7 was these-held The number of the edges of the binary-ized signal S3 corresponding to the rising edge of the oscillation output signal S6 and the number of the edges of the binary-ized signal S3 corresponding to the falling edge of the oscillation output signal S6 are totaled. Moreover, the amount of gaps of an edge is similarly totaled and average-ized for every standup of the oscillation output signal S6, and falling.

[0058] The statistic count circuit 47 chooses the total result of the amount of edge gaps of the direction with many edges from the number of the edges which did in this way and totaled, and the oscillation output signal S6 judges a leading phase or a delay phase from this total result to the edge corresponding to a binary-ized signal. From this judgment result, the statistic count circuit 47 outputs a control signal S8 to the adjustable mold counting-down circuit 44, and carries out adjustable [of the division ratio of the adjustable mold counting-down circuit 44] per 1 dividing.

[0059] Thereby, the statistic count circuit 47 calculates the amount of phase shifts of the oscillation output signal S6 corresponding to the rising edge or falling edge of the binary-ized signal S3 which comes to have much edge information based on a phase comparison result, and it constitutes a phase comparison result processing means to the extent that it carries out adjustable [of the frequency of the oscillation output signal S6] from this amount of phase shifts.

[0060] Thereby, an oscillator 43, the adjustable mold counting-down circuit 44, two counting-down circuits 45, the amount detector 46 of edge location gaps, and the statistic count circuit 47 constitute a PLL circuit, its timing of an edge corresponds to the rising edge or falling edge of the binary-ized signal S3, and the oscillation output signal S6 which comes to carry out phase simulation according to predetermined phase contrast to the clock of the PSK modulating signal S1 is generated (drawing 5 (E) and (F)).

[0061] Furthermore, the statistic count circuit 47 outputs count result S9 of the amount of phase shifts of another side which offers and remains in the output of a control signal S8 to the sampling position count circuit 48. In addition, the latch group which the statistic count circuit 47 incorporates selectively the logical level detected in the amount detector 46 of edge location gaps, respectively to each edge of the oscillation output signal S6, and the timing before and behind each edge, and carries out a sequential transfer, It is constituted by the adder circuit adding the output of these latch group,

and the comparison circuit which compares the addition result of these adder circuits. It is made as [output / output this comparison result selectively, and output a control signal S8 to the adjustable mold counting-down circuit 44, and / to the sampling position count circuit 48 / count result S9].
[0062] Based on this count result S9, by delaying the oscillation output signal S6, the sampling position count circuit 48 amends gradually the phase contrast of the oscillation output signal S6 over the clock of the PSK modulating signal S1, and outputs Clock CK.
[0063] A latch circuit 49 restores to them and outputs data streams D (R->C) and D (C->R) by carrying out the sequential latch of the binary-ized signal S3 on the basis of this clock CK.
[0064] In the above configuration, the main carrier Sm of a frequency Fm becomes irregular, and the IC card system 11 is sent out from a loop antenna 18, after the PSK modulation of the transmit data train D (R->C) sent out to IC card 12 from (drawing 2 and drawing 3), and the lead writer 13 is carried out by the clock CK 1 of a frequency F1 with a modulator 27.
[0065] If IC card 12 approaches the lead writer 13 by this, induction of the sending signal which this main carrier Sm comes to become irregular will be carried out to the loop antenna 14 of IC card 12. A part is changed into the power of IC card 12 by the current supply circuit 29, and the strange demodulator circuit 15 of IC card 12 and a digital disposal circuit 16 drive this sending signal by which induction was carried out with this power.
[0066] The output signal S1 of a modulator 27 gets over with a demodulator 32, after this signal component is band-limited by the band pass filter 33 and separated with other signal components, the sending signal furthermore obtained from this loop antenna 14 is inputted into the continuing demodulator 34, and the transmit data train D (R->C) restores to it here.
[0067] By this, this transmit data train D (R->C) is analyzed by the digital disposal circuit 16, response data stream D (C->R) sent out to the lead writer 13 is generated, and this response data stream D (C->R) is inputted into a modulator 35. This response data stream D (C->R) is sent out from a loop antenna 14 as an amplitude-modulated signal of the main carrier Sm of a sending signal here by carrying out adjustable [of the load impedance of a loop antenna 14] by the PSK modulating signal S2 which was modulated with the clock CK 2 of a frequency F2, and was generated with this modulator 35.
[0068] Thereby, response data stream D (C->R) is transmitted to the lead writer 13 from IC card 12. Thus, it is received by the lead writer 13 by a loop antenna 14 and the loop antenna 18 to combine, the reply signal which becomes by this received signal is inputted into a demodulator 38, and, thereby, the output signal S2 of a modulator 35 restores to transmitted response data stream D (C->R). After dissociating with other signal components by furthermore band-limiting this signal component with a band pass filter 39, it is inputted into the continuing demodulator 40 and response data stream D (C->R) gets over here.
[0069] Thus, when an PSK modulation is carried out with the clocks CK1 and CK2 of frequencies F1 and F2, it is transmitted by bit coding by the Manchester code (drawing 5) and it gets over by IC card 12 and the lead writer 13, respectively, waveform distortion generates the transmit data train D (R->C) sent and received and response data stream D (C->R) in the PSK modulating signals S1 and S2 with the distance of IC card 12 and the lead writer 13.
[0070] These received PSK modulating signals S1 and S2 will be made binary in the binary-ized circuit 42 by the simple configuration of (drawing 1) and limiter circuitry, and a duty ratio will change with the distance of IC card 12 and the lead writer 13 a lot in the binary-ized signal S3 by this, and logical level will change with noises.
[0071] In demodulators 34 and 40, in an oscillator 43, oscillation output signal S4 by the twice [predetermined] as many square wave signal as this is generated to the frequency F1 of the clock CK 1 of the PSK modulating signal S1, dividing of this oscillation output signal S4 is carried out with the adjustable mold counting-down circuit 44, and the oscillation output signal S5 of the square wave by the twice [about] as many frequency as this is generated to the clock CK 1 of the PSK modulating signal S1. Moreover, 1 / 2 dividing of this oscillation output signal S5 are carried out by two counting-down circuits 45, and the oscillation output signal S6 of the clock CK 1 of the PSK modulating signal S1 and a square wave with an almost equal frequency is generated.
[0072] In the amount detector 46 of edge location gaps, it is the range of 1/2 period centering on each edge of the oscillation output signal S6, and, as for the binary-ized signal S3, a leading phase or

a delay phase is detected to the existence of an edge, and the edge of the oscillation output signal S6 by the phase comparison with this oscillation output signal S5. In the statistic count circuit 47 which furthermore continues, the number of the edges of the binary-ized signal S3 corresponding to the rising edge of the oscillation output signal S6 and the number of the edges of the binary-ized signal S3 corresponding to the falling edge of the oscillation output signal S6 are totaled by the statistics processing on the basis of the oscillation output signal S6, and the amount of gaps of an edge is similarly totaled for every standup of the oscillation output signal S6, and falling.
[0073] The division ratio of the adjustable mold counting-down circuit 44 is switched one by one so that the total result of the amount of edge gaps of the direction with many edges is chosen from the number of the edges which furthermore totaled, a leading phase or a delay phase may be judged for the oscillation output signal S6 to the edge to which the binary-ized signal S3 corresponds from this total result and this phase shift may be amended. Phase control of the oscillation output signal S6 is carried out so that the rising edge or falling edge of the oscillation output signal S6 may carry out phase simulation to the edge of the binary-ized signal S3 by this.
[0074] It is delayed in the sampling position count circuit 48 by count result S9 of the amount of phase shifts of another side where the oscillation output signal S6 which comes to carry out phase control by doing still in this way offers and remains in the output of a control signal S8. The clock CK which comes to carry out phase simulation to the clock CK 1 of the PSK modulating signal S1 by this is generated, the sequential latch of the binary-ized signal S3 is carried out with this clock CK, and data stream D (R->C) gets over.
[0075] Even when it was controlled so that one edge of the oscillation output signal S6 carried out phase simulation to the binary-ized signal S3 by this, and the phase contrast of the edge of another side amends the timing of this oscillation output signal S6, Clock CK is generated and the duty ratio of the binary-ized signal S3 changes, Clock CK is reproduced correctly.
[0076] By choosing the total result of the amount of edge gaps of the direction with many edges furthermore at this time, and controlling the phase of the oscillation output signal S6 to the edge to which the binary-ized signal S3 corresponds from this total result Like [in the case of being based on a Manchester code], one clock is made into a unit, a phase is reversed, and even if the case where the logical level of modulating signals S1 and S2 does not switch synchronizing with Clock CK occurs, Clock CK is reproduced certainly. Moreover, by totaling and processing the amount of edge gaps at this time, the effect of a noise is avoided effectively.
[0077] Even when the duty ratio of the binary-ized signal S3 changes by controlling the frequency of the oscillation output signal S6 so that one edge of the oscillation output signal S6 carries out phase simulation to the binary-ized signal S3, and the phase contrast of the edge of another side amending the timing of this oscillation output signal S6, and generating Clock CK according to the above configuration, Clock CK can be reproduced correctly. Moreover, by totaling and average-izing the amount of edge gaps, the effect of a noise is effectively avoidable. The distance between an IC card and a lead writer changes with these, and even when the PSK modulating signal which becomes with an input signal deteriorates, an input signal can be certainly processed with a simple configuration.
[0078] (2) Gestalt drawing 6 of the 2nd operation is the block diagram showing the demodulator applied to the IC card and IC card processor concerning the gestalt of the 2nd operation. In the configuration shown in this drawing 6 , the same configuration as the demodulator mentioned above about drawing 1 attaches a corresponding sign, it is shown and the duplicate explanation is omitted.
[0079] In this demodulator 50, the binary-ized circuit 51 makes the PSK modulating signal S1 binary, and outputs that binary-ized signal S3A and binary-ized signal S3B which comes to be reversed of the polarity of this binary-ized signal S3A.
[0080] The adjustable mold counting-down circuit 52 carries out dividing of the oscillation output signal S4 of an oscillator 43, and outputs 2nd oscillation output signal S6I from which a phase differs about 90 degrees to the PSK modulating signal S1, 1st oscillation output signal S6Q with an almost equal frequency, and this 1st oscillation output signal S6Q.
[0081] selector 53Q -- criteria [Q / 1st / oscillation output signal S6] -- carrying out -- binary-izing -- by outputting signal S3A and S3B selectively, phase comparison result S7Q is outputted to the extent that it is the same in having carried out the phase comparison of 1st oscillation output signal S6Q and the binary-ized signal S3A by the exclusive OR.

[0082] selector 53I -- criteria [I / 2nd / oscillation output signal S6] -- carrying out -- binary-izing -- by outputting signal S3A and S3B selectively, phase comparison result S7I is outputted to the extent that it is the same in having carried out the phase comparison of 2nd oscillation output signal S6I and the binary-ized signal S3B by the exclusive OR.
[0083] Low pass filter (LPF) 54Q obtains the moving average of phase comparison result S7Q, and outputs this moving average deviation as a recovery result. Low pass filter (LPF) 54I outputs the moving average of phase comparison result S7I.
[0084] The control direction judging circuit 55 determines the adjustable direction of the division ratio in the adjustable mold counting-down circuit 52 on the basis of the output signal of low pass filters 54Q and 54I, and outputs a control signal S8 according to this adjustable direction.
[0085] Namely, if analog quantity S7IA and S7QA show a phase comparison result to the extent that comparison with phase comparison result S7I and S7Q twists to the exclusive OR between clocks CK 1 as shown in drawing 7 the time (at phase contrast 0 and the time of pi/2) of the phase being in agreement to a clock CK 1 -- about -- a respectively big value is acquired, and in a phase comparison result, as for phase comparison result S7I and S7Q, a phase comparison result is obtained at least for that of a value 0 to the extent that phases differ about 90 degrees at this time. Furthermore, these values change with change of phase contrast in the shape of a triangular waveform (drawing 7 (A) and (B)).
[0086] If the sign of phase comparison result S7I and S7Q shows at least this relation (drawing 7 (C) and (D)), a value will just start in -90 to 90 degrees, and a value will fall [in / at least in that / 2nd / phase comparison result S7I] to negative the range of -90 to -180 degrees, and in 90 to 180 degrees. Moreover, a value just starts in 0 times to 90 degrees, and a value falls [in / at least in that / 1st / in which a phase differs from this about 90 degrees / phase comparison result S7Q] from 0 times to negative in -180 degrees.
[0087] Thereby, the sign of phase comparison result S7I and S7Q shows that the phase shift to binary-ized signal S3A is roughly detectable.
[0088] On the other hand, in the Manchester code which becomes on the generation criteria of binary-ized signal S3A, the phase of 0 times and 180 degrees is formed to Clock CK according to the logical level of data. In this case, in phase comparison result S7I and S7Q, the part which carries out phase simulation to a clock CK 1 will switch by zero phase contrast and 180 phase contrast according to the data transmitted by the PSK modulating signal S1 to the extent that binary-ized signal S3A was used.
[0089] thereby -- to the extent that -- an arrow head a shows the range whose phase contrast detected by phase comparison result S7I is -90 - 90 degrees -- as -- about -- the phase contrast of phase comparison result S7Q becomes 0 times -- as -- controlling -- about -- oscillation output signal S6I which becomes on the generation criteria of phase comparison result S7I can be synchronized with Clock CK.
[0090] moreover -- about -- an arrow head b shows the range whose phase contrast detected by phase comparison result S7I is -180 - -90 degrees and 90 - 180 degrees -- as -- about -- the phase contrast of phase comparison result S7Q becomes 180 degrees -- as -- controlling -- about -- oscillation output signal S6I which becomes on the generation criteria of phase comparison result S7I can be synchronized with Clock CK.
[0091] According to this relation, as shown in drawing 8 , the control direction judging circuit 55 holds the table which made the address the sign of phase comparison result S7I and S7Q, determines the control direction on this table, and outputs a control signal S8 according to this control direction. In addition, in this drawing 8 , + and - show the control direction here.
[0092] According to the configuration shown in drawing 6 , even when at least those [these / 1st and 2nd] determined the control direction according to the positive/negative of a phase comparison result, and carried out adjustable [of oscillation frequency] and the PSK modulating signals S1 and S2 deteriorate with a simple configuration, at least those [1st and 2nd] by the oscillation output signal with which phases differ about 90 degrees can reproduce Clock CK certainly, and can recover data from a phase comparison result.
[0093] (3) Gestalt drawing 9 of the 3rd operation is the block diagram showing the demodulator concerning the gestalt of the 3rd operation. It replaces with the selectors 53Q and 53I mentioned

above in drawing 6 , and, as for this demodulator 60, at least the IKUSUKURUSHIBUOA circuits (EX-OR) 61Q and 61I detect phase comparison result S7Q and S7I.

[0094] The switch circuit 62 judges whether 1st [corresponding to the output of low pass filters 54Q and 54I] and 2nd oscillation output signal S6Q and which phase of S6I are close to the phase of Clock CK by absolute-value-izing the output of low pass filters 54Q and 54I, and measuring it. Furthermore, from this decision result, the output of the inputted low pass filters 54Q and 54I is replaced, and it outputs to the control direction judging circuit 55.

[0095] Thereby, in drawing 10 , the switch circuit 62 is made as [carry out / at high speed / at the time of a switch and its part standup / the phase simulation of phase comparison result S7I and the S7Q] so that I arm may show and the phase of the PSK modulating signal S1 may approach [phase / by 1st oscillation output signal S6Q] the phase of any or a near side in the phase of Q arm and 2nd oscillation output signal S6I.

[0096] according to the configuration shown in drawing 9 -- the 3rd configuration of the gestalt of operation -- in addition, the phase of the PSK modulating signal S1 approaches the phase of any or a near side -- as -- about -- switching phase comparison result S7I and S7Q -- the effectiveness of the gestalt of the 2nd operation -- in addition, phase simulation can be carried out at high speed at the time of a standup.

[0097] (4) it is the gestalt of other operations -- in the gestalt of the above-mentioned 2nd and the 3rd operation, although the case where a recovery result was outputted from the output of a low pass filter was described, this invention may latch a binary-ized signal by the latch circuit separately in addition to this, and may output a recovery result.

[0098] Furthermore, although the case where an IC card was operated with the power of a sending signal in the gestalt of above-mentioned operation was described, when operating this invention not only by this but by the cell, it can be applied widely.

[0099] Moreover, although the case where generated a clock from the PSK modulating signal by the Manchester code, and it restored to data in the gestalt of above-mentioned operation was described, this invention can be widely applied, when generating a clock from various modulating signals when not only this but various PSK modulating signals generate a clock, and it restores to data and it generates a clock from an ASK modulating signal further, and reproducing data using this clock.

[0100] Moreover, in the gestalt of above-mentioned operation, although the case where this invention was applied to the lead writer which becomes with an IC card and an IC card processor was described, this invention is widely applicable to the PLL circuit of not only this but various data transmission units, and a demodulator circuit.

[0101]

[Effect of the Invention] The amount of phase shifts to which at least that of an oscillation output signal and a binary-ized signal average-value-izes a phase comparison result selectively, and receives as mentioned above any of a rising edge or a falling edge they are according to this invention is calculated. controlling an oscillation output signal from this amount of phase shifts -- moreover, with a simple configuration by determining the control direction on the basis of the positive/negative of a phase comparison result to the extent that it is based on the oscillation output signal with which phases differ about 90 degrees, and controlling an oscillation output signal in this control direction Even when an input signal deteriorates, an input signal can be processed certainly.

[Translation done.]

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CLAIMS

[Claim(s)]

[Claim 1] In the PLL circuit which reproduces the clock of said input signal from the input signal transmitted through the desired transmission system A binary-ized means to make said input signal binary and to generate a binary-ized signal, and the signal generation means which carries out adjustable [of the frequency of an oscillation output signal] with a control signal, A phase-comparison means to carry out the phase comparison of said oscillation output signal and said binary-ized signal, and to output a phase comparison result, The 1st amount of phase shifts of said binary-ized signal [as opposed to / at least the above average-value-izes a phase comparison result selectively, and / the rising edge of said oscillation output signal], To the extent that the 2nd amount of phase shifts of said binary-ized signal over the falling edge of said oscillation output signal is calculated and said control signal is outputted from said 1st or 2nd amount of phase shifts A phase comparison result processing means, The PLL circuit characterized by having a phase correction means to amend the phase of said oscillation output signal and to output said clock, based on the detection result of said 2nd or 1st amount of phase shifts.

[Claim 2] The PLL circuit according to claim 1 characterized by said input signal becoming with an PSK modulating signal.

[Claim 3] The PLL circuit according to claim 1 characterized by said input signal becoming with the modulating signal by the Manchester code.

[Claim 4] In the demodulator circuit which reproduces the data stream transmitted through said input signal from the input signal transmitted through the desired transmission system A binary-ized means to make said input signal binary and to generate a binary-ized signal, and the signal generation means which carries out adjustable [of the frequency of an oscillation output signal] with a control signal, A phase-comparison means to carry out the phase comparison of said oscillation output signal and said binary-ized signal, and to output a phase comparison result, The 1st amount of phase shifts of said binary-ized signal [as opposed to / at least the above average-value-izes a phase comparison result selectively, and / the rising edge of said oscillation output signal], To the extent that the 2nd amount of phase shifts of said binary-ized signal over the falling edge of said oscillation output signal is calculated and said control signal is outputted from said 1st or 2nd amount of phase shifts A phase comparison result processing means, The demodulator circuit characterized by having a timing amendment means to amend the phase of said oscillation output signal and to output a timing amendment signal, and a latch means to latch said binary-ized signal with said timing amendment signal, based on the detection result of said 2nd or 1st amount of phase shifts.

[Claim 5] The demodulator circuit according to claim 4 characterized by said input signal becoming with an PSK modulating signal.

[Claim 6] The demodulator circuit according to claim 4 characterized by said input signal becoming with the modulating signal by the Manchester code.

[Claim 7] In the IC card which restores to a data stream by the demodulator circuit, and is processed from the sending signal received through the antenna said demodulator circuit A binary-ized means to make binary the modulating signal acquired from said sending signal, and to generate a binary-ized signal, A phase-comparison means to carry out the phase comparison of the signal generation means which carries out adjustable [of the frequency of an oscillation output signal] with a control signal, and said oscillation output signal and said binary-ized signal, and to output a phase comparison result, The 1st amount of phase shifts of said binary-ized signal [as opposed to / at least the above average-value-izes a phase comparison result selectively, and / the rising edge of said oscillation output signal], To the extent that the 2nd amount of phase shifts of said binary-ized signal over the falling edge of said oscillation output signal is calculated and said control signal is outputted from said 1st or 2nd amount of phase shifts A phase comparison result processing means, A timing amendment means to amend the phase of said oscillation output signal and to output a timing amendment signal based on the detection result of said 2nd or 1st amount of phase shifts, The IC card characterized by having a latch means to latch said binary-ized signal with said timing amendment signal, and to reproduce said data stream.

[Claim 8] The IC card according to claim 7 characterized by said modulating signal becoming with an PSK modulating signal.

[Claim 9] The IC card according to claim 7 characterized by said modulating signal becoming by the signal by the Manchester code.

[Claim 10] In the IC card processor which restores to it and processes the data stream sent out from the IC card using the demodulator circuit from the reply signal received through the antenna said demodulator circuit A binary-ized means to make binary the modulating signal acquired from said reply signal, and to generate a binary-ized signal, A phase-comparison means to carry out the phase comparison of the signal generation means which carries out adjustable [of the frequency of an oscillation output signal] with a control signal, and said oscillation output signal and said binary-ized signal, and to output a phase comparison result, The 1st amount of phase shifts of said binary-ized signal [as opposed to / at least the above average-value-izes a phase comparison result selectively, and / the rising edge of said oscillation output signal], To the extent that the 2nd amount of phase shifts of said binary-ized signal over the falling edge of said oscillation output signal is calculated and said control signal is outputted from said 1st or 2nd amount of phase shifts A phase comparison result processing means, A timing amendment means to amend the phase of said oscillation output signal and to output a timing amendment signal based on the detection result of said 2nd or 1st amount of phase shifts, The IC card processor characterized by having a latch means to latch said binary-ized signal with said timing amendment signal, and to reproduce said data stream.

[Claim 11] The IC card processor according to claim 10 characterized by said modulating signal becoming with an PSK modulating signal.

[Claim 12] The IC card processor according to claim 10 characterized by said modulating signal becoming by the signal by the Manchester code.

[Claim 13] In the PLL circuit which reproduces the clock of said input signal from the input signal transmitted through the desired transmission system It carries out adjustable [of the frequency] to a binary-ized means to make said input signal binary and to generate a binary-ized signal, with a control signal. A signal generation means to output the 2nd oscillation output signal with which phases differ about 90 degrees to the 1st oscillation output signal and said 1st oscillation output signal, 1st phase-comparison means by which carry out the phase comparison of said the 1st oscillation output signal and said binary-ized signal, and at least that [1st] outputs a phase comparison result, 2nd phase-comparison means by which carry out the phase comparison of said the 2nd oscillation output signal and said binary-ized signal, and at least that [2nd] outputs a phase comparison result, The PLL circuit characterized by having the control means by which at least those [said / 1st and 2nd] determines the control direction based on the positive/negative of a phase comparison result, outputs said control signal based on said control direction, and controls actuation of said signal generation means.

[Claim 14] The PLL circuit according to claim 13 characterized by said input signal becoming with an PSK modulating signal.

[Claim 15] The PLL circuit according to claim 13 characterized by said input signal becoming with the modulating signal by the Manchester code.

[Claim 16] It is the PLL circuit according to claim 13 characterized by for said signal generation means carrying out dividing of the predetermined reference signal by the predetermined division ratio, outputting said 1st and 2nd oscillation output signals, and for said control means switching said division ratio gradually one by one with said control signal, and controlling actuation of said signal

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generation means.
[Claim 17] Said control means is a PLL circuit according to claim 13 where at least those [said / 1st and 2nd] is characterized by at least those [said / 1st and 2nd] determining the switch aforementioned control direction for a phase comparison result based on a phase comparison result.
[Claim 18] In the demodulator circuit which reproduces the data stream transmitted through said input signal from the input signal transmitted through the desired transmission system It carries out adjustable [of the frequency] to a binary-ized means to make said input signal binary and to generate a binary-ized signal, with a control signal. A signal generation means to output the 2nd oscillation output signal with which phases differ about 90 degrees to the 1st oscillation output signal and said 1st oscillation output signal, 1st phase-comparison means by which carry out the phase comparison of said the 1st oscillation output signal and said binary-ized signal, and at least that [1st] outputs a phase comparison result, 2nd phase-comparison means by which carry out the phase comparison of said the 2nd oscillation output signal and said binary-ized signal, and at least that [2nd] outputs a phase comparison result, At least those [said / 1st and 2nd] determines the control direction based on the positive/negative of a phase comparison result. The demodulator circuit characterized by having the control means which outputs said control signal based on said control direction, and controls actuation of said signal generation means, and at least that [said / 1st or 2nd] outputting said data stream by the phase comparison result.
[Claim 19] The demodulator circuit according to claim 18 characterized by said input signal becoming with an PSK modulating signal.
[Claim 20] The demodulator circuit according to claim 18 characterized by said input signal becoming with the modulating signal by the Manchester code.
[Claim 21] It is the demodulator circuit according to claim 18 characterized by for said signal generation means carrying out dividing of the predetermined reference signal by the predetermined division ratio, outputting said 1st and 2nd oscillation output signals, and for said control means switching said division ratio gradually one by one with said control signal, and controlling actuation of said signal generation means.
[Claim 22] Said control means is a demodulator circuit according to claim 18 where at least those [said / 1st and 2nd] is characterized by at least for those [said / 1st and 2nd] switching a phase comparison result, and determining said control direction based on a phase comparison result.
[Claim 23] In the IC card which restores to a data stream by the demodulator circuit, and is processed from the sending signal received through the antenna said demodulator circuit It carries out adjustable [of the frequency] to a binary-ized means to make said sending signal binary and to generate a binary-ized signal, with a control signal. A signal generation means to output the 2nd oscillation output signal with which phases differ about 90 degrees to the 1st oscillation output signal and said 1st oscillation output signal, 1st phase-comparison means by which carry out the phase comparison of said the 1st oscillation output signal and said binary-ized signal, and at least that [1st] outputs a phase comparison result, 2nd phase-comparison means by which carry out the phase comparison of said the 2nd oscillation output signal and said binary-ized signal, and at least that [2nd] outputs a phase comparison result, At least those [said / 1st and 2nd] determines the control direction based on the positive/negative of a phase comparison result. The IC card characterized by having the control means which outputs said control signal based on said control direction, and controls actuation of said signal generation means, and at least that [said / 1st or 2nd] outputting said data stream by the phase comparison result.
[Claim 24] The IC card according to claim 23 characterized by said sending signal becoming with an PSK modulating signal.
[Claim 25] The IC card according to claim 23 characterized by said sending signal becoming with the modulating signal by the Manchester code.
[Claim 26] It is the IC card according to claim 23 characterized by for said signal generation means carrying out dividing of the predetermined reference signal by the predetermined division ratio, outputting said 1st and 2nd oscillation output signals, and for said control means switching said division ratio gradually one by one with said control signal, and controlling actuation of said signal generation means.
[Claim 27] Said control means is an IC card according to claim 23 with which at least those [said / 1st and 2nd] is characterized by at least for those [said / 1st and 2nd] switching a phase comparison

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result, and determining said control direction based on a phase comparison result.

[Claim 28] In the IC card processor which restores to it and processes the data stream sent out from the IC card using the demodulator circuit from the reply signal received through the antenna said demodulator circuit It carries out adjustable [of the frequency] to a binary-ized means to make said reply signal binary and to generate a binary-ized signal, with a control signal. A signal generation means to output the 2nd oscillation output signal with which phases differ about 90 degrees to the 1st oscillation output signal and said 1st oscillation output signal, 1st phase-comparison means by which carry out the phase comparison of said the 1st oscillation output signal and said binary-ized signal, and at least that [1st] outputs a phase comparison result, 2nd phase-comparison means by which carry out the phase comparison of said the 2nd oscillation output signal and said binary-ized signal, and at least that [2nd] outputs a phase comparison result, At least those [said / 1st and 2nd] determines the control direction based on the positive/negative of a phase comparison result. The IC card processor characterized by having the control means which outputs said control signal based on said control direction, and controls actuation of said signal generation means, and at least that [said / 1st or 2nd] outputting said data stream by the phase comparison result.

[Claim 29] The IC card processor according to claim 28 characterized by said reply signal becoming with an PSK modulating signal.

[Claim 30] The IC card processor according to claim 28 characterized by said reply signal becoming with the modulating signal by the Manchester code.

[Claim 31] It is the IC card processor according to claim 28 characterized by for said signal generation means carrying out dividing of the predetermined reference signal by the predetermined division ratio, outputting said 1st and 2nd oscillation output signals, and for said control means switching said division ratio gradually one by one with said control signal, and controlling actuation of said signal generation means.

[Claim 32] Said control means is an IC card processor according to claim 28 with which at least those [said / 1st and 2nd] is characterized by at least for those [said / 1st and 2nd] switching a phase comparison result, and determining said control direction based on a phase comparison result.

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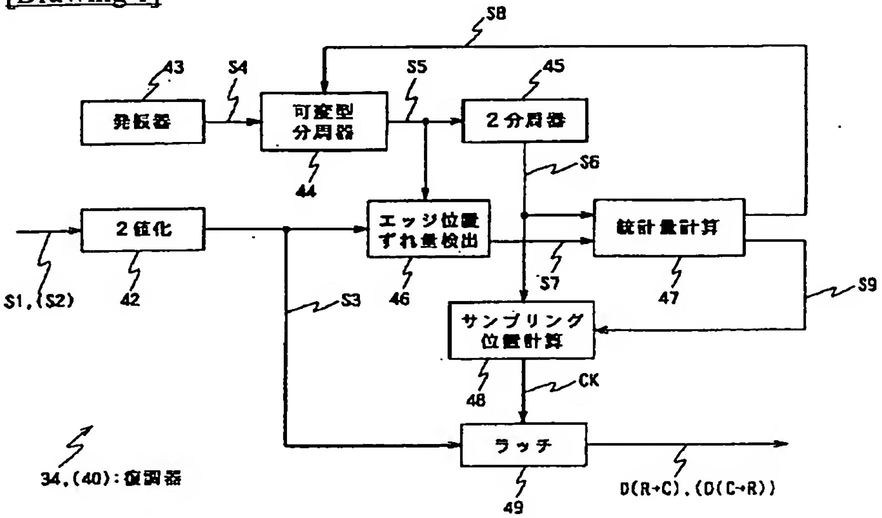
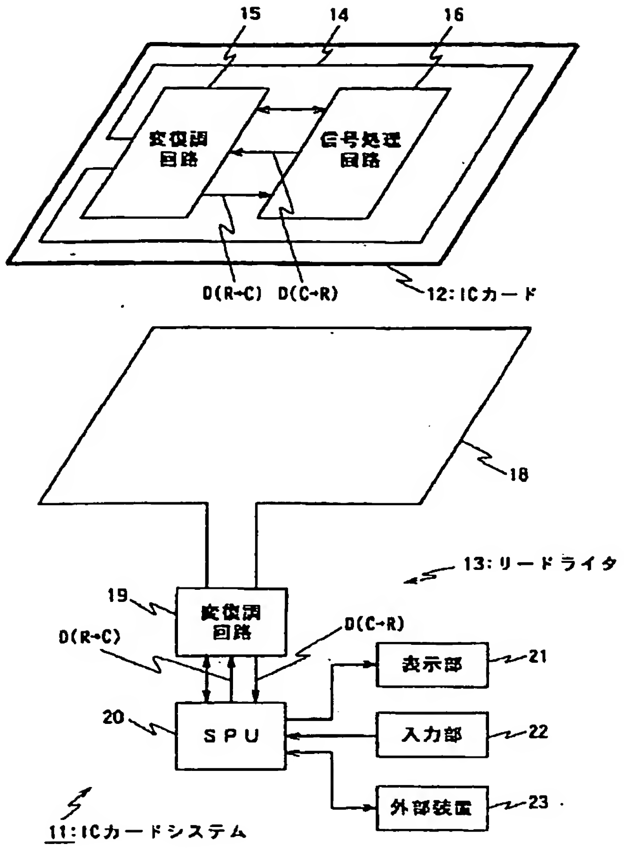
DRAWINGS

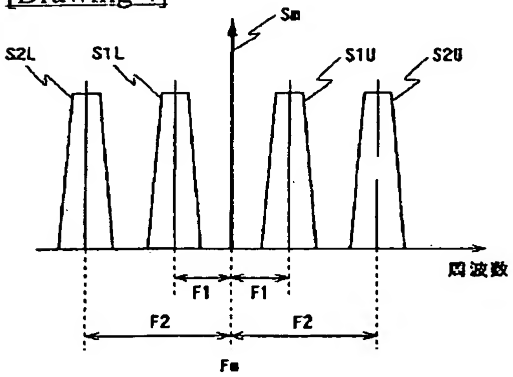
[Drawing 1]


S8
43
S4
S5
45
発振器
可変型分周器
2分周器
44
S6
2値化
エッジ位置ずれ量検出
統計量計算
S1,(S2)
42
S3
46
S7
47
S9
サンプリング位置計算
48
CK
ラッチ
34,(40):復調器
49
D(R→C),(D(C→R))

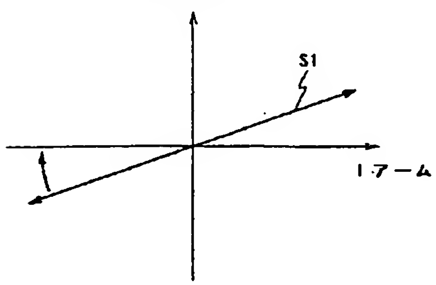
[Drawing 2]


15
14
16
変復調回路
信号処理回路
D(R→C)
D(C→R)
12: ICカード
18
13: リードライタ
19
変復調回路
D(R→C)
D(C→R)
20
SPU
表示部
21
入力部
22
外部装置
23
11: ICカードシステム

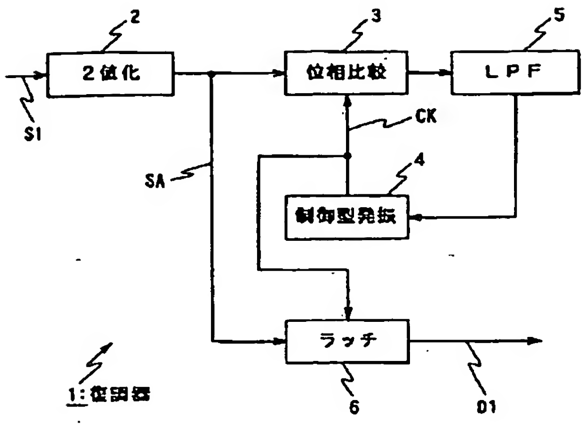
[Drawing 4]


Sm
S2L
S1L
S1U
S2U
周波数
F1
F1
F2
F2
Fm

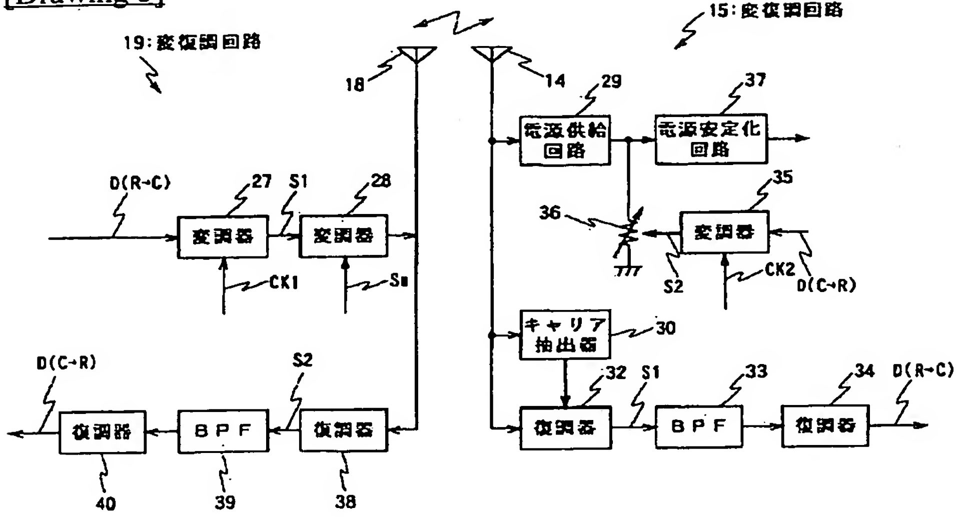
[Drawing 10]


Qアーム
S1
Iアーム

[Drawing 11]


2
3
5
2値化
位相比較
LPF
S1
CK
SA
4
制御型発振
ラッチ
1:復調器
6
D1

[Drawing 3]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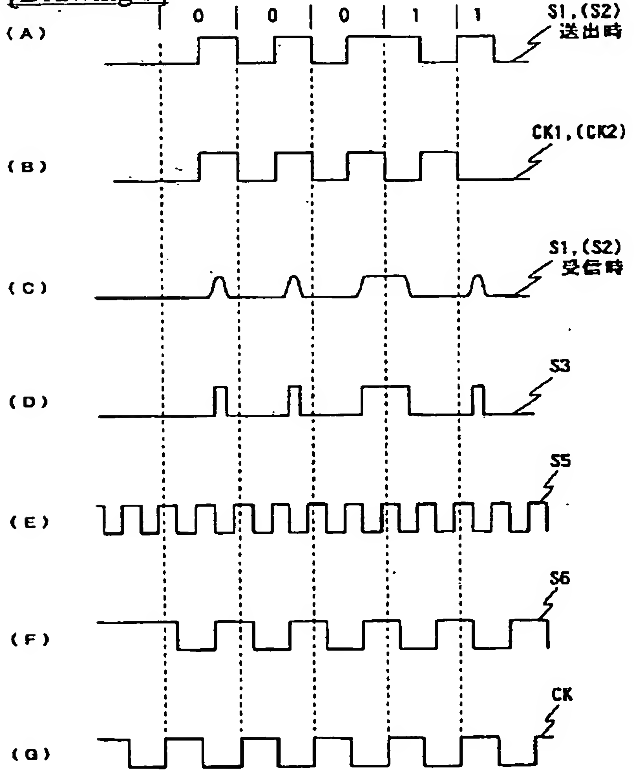
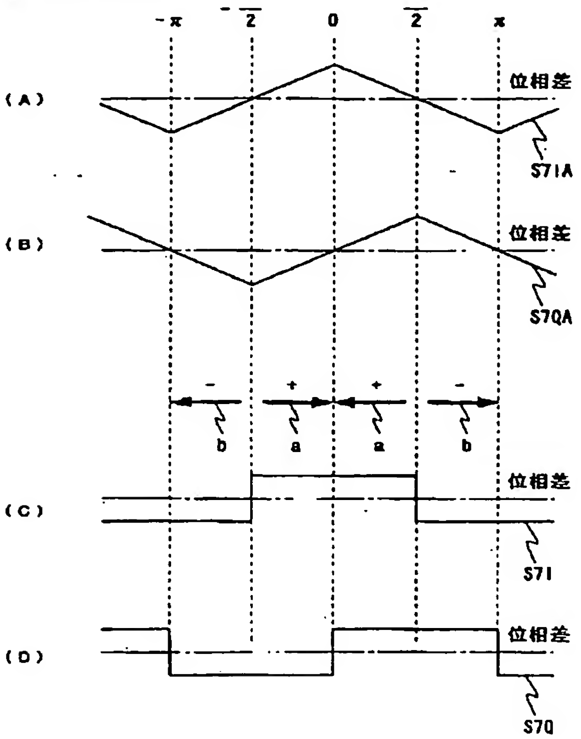
19:変復調回路
18
14
29
37
電源供給回路
電源安定化回路
D(R→C)
27
S1
28
35
36
変調器
変調器
変調器
CK1
S4
S2
CK2
D(C→R)
キャリア抽出器
30
D(C→R)
S2
32
S1
33
34
D(R→C)
復調器
BPF
復調器
復調器
BPF
復調器
40
39
38

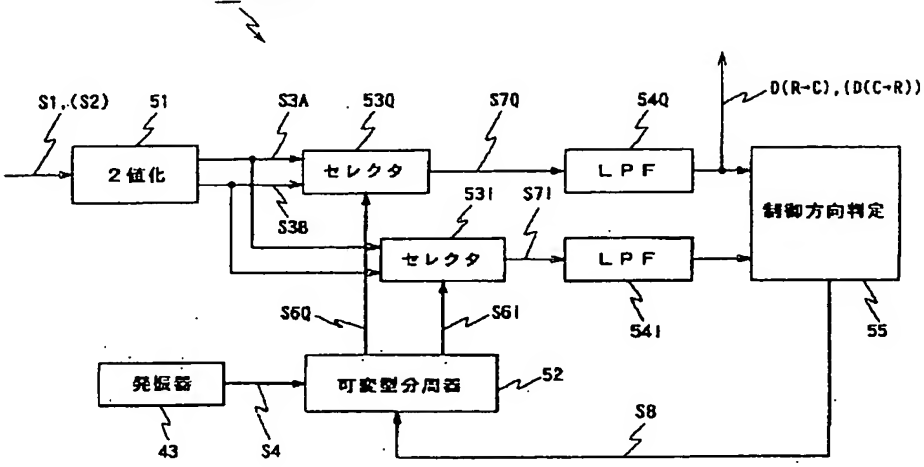
[Drawing 5]



[Drawing 7]


-π
-π/2
0
π/2
π
(A)
位相差
S7IA
(B)
位相差
S7QA
-
+
+
-
b
a
a
b
(C)
位相差
S7I
(D)
位相差
S7Q

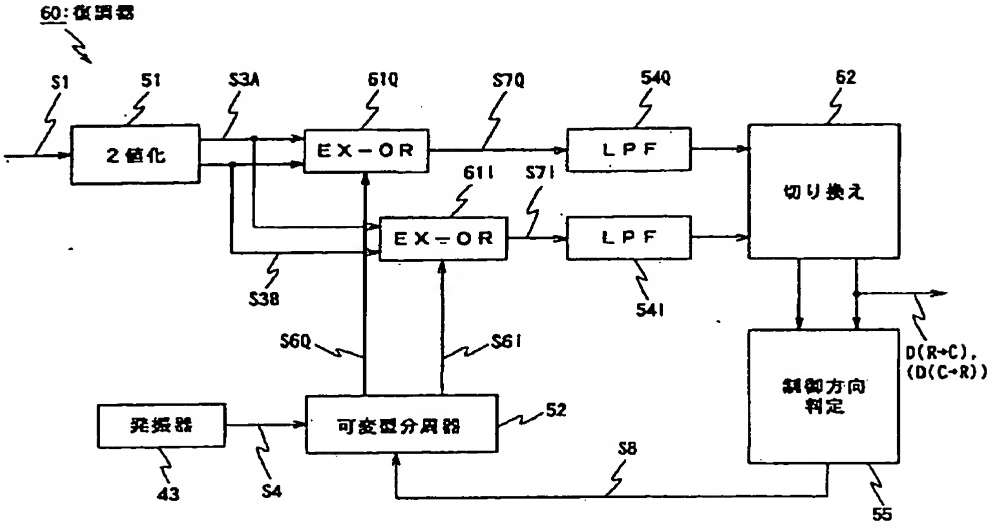
[Drawing 6]


50:復調器
S1,(S2)
51
2値化
S3A
S3B
53Q
セレクタ
53I
セレクタ
S7Q
S7I
54Q
LPF
LPF
54I
D(R→C),(D(C→R))
制御方向判定
55
S6Q
S6I
発振器
43
S4
可変型分周器
52
S8

[Drawing 8]

位相ずれ	-π		-1/2π		0		1/2π		π
S7I	-	-	0	+	+	+	0	-	-
S7Q	0	-	-	-	0	+	+	+	0
制御方向	0	+	-	-	0	+	+	-	0

[Drawing 9]


60:復調器
S1
51
2値化
S3A
S3B
61Q
EX−OR
61I
EX−OR
S7Q
S7I
LPF
LPF
54Q
54I
62
切り換え
制御方向判定
D(R→C),
(D(C→R))
S6Q
S6I
発振器
43
S4
可変型分周器
52
S8
55

[Translation done.]